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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,013	02/08/2002	Gang Zha	00-SZ-106	8843

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EXAMINER	
MOTTOLA, STEVEN J	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 09/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
07/101 3	Zha, Ng
Examiner	**Group Art Unit**
Mottola	2817

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☑ Responsive to communication(s) filed on August 4, 2003.

☑ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☑ Claim(s) 1-15 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☑ Claim(s) 10-13 is/are allowed.

☑ Claim(s) 1-4 & 14 is/are rejected.

☑ Claim(s) 5-9 & 15 is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received: _____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Notice of Reference(s) Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

Office Action Summary

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Fattaruso.

Refer to fig. 7 of Fattaruso. An input differential pair M11,M12 may be read as the input stage of claim 1, with M11,M12 read as the first and second transistors of claim 2. Transistors Mf1,M21 each generate an output signal and may be read as the output stage of claim 1. The signal from M21 may be read as the second feedback signal since it is fed back via capacitor 16. Then current mirror stage M13,M14 may be read as the gain stage of claim 1. It is connected to both the input and output stages as defined above and an equal "current potential" should be available at stage outputs CN1,CN2 as long as the transistors are matched. Regarding claim 2, the transistors M11,M12 are read as the first and second transistors claimed as noted above, and they are connected as claimed in the last paragraph of the claim. Current source I1 of Fattaruso may be read as the like element claimed. Regarding claims 3-4, transistors M13,M14 form a current mirror as claimed and may be read as the third and fourth transistors claim 3 or the first and second transistors of claim 4. They are connected as in the last paragraph of the claim. In re claim 14, the input, output and gain stages may be read on the reference in the same manner as for claim 1 above. A voltage potential Vdd-Vss is applied across the amplifier as claimed. Regarding the

resistive element claimed to be between the first output and a voltage potential, in Fattaruso the first output would be read on the drain of Mf1 and it is connected to a potential Vdd via an enhancement mode FET M23 which is a "resistive element" as claimed in that it has a channel conductance; see col. 6, last paragraph of Fattaruso. Note that a certified translation of the supplied priority document would remove the 'bar' under 35 U.S.C. 102(b) , but that the reference would still be applicable under 35 U.S.C. 102(e).

Regarding the arguments presented against the above rejection, while the amplifier of the present invention receives a single ended input signal this is not positively recited in the claims and the inputs IN10,IN11 to Fattaruso may properly be refered to as 'an input signal' albeit a differential signal. Even if they were regarded as two separate signals, this would not be excluded by the claims. Although Fattaruso refers to Mf1 as a feedforward stage, its output is mirrored to the output terminal and thus it does supply an output signal, so it is being read as one of the transistors of the claimed output stage. The fact that this output is combined with the other output from M21 is not excluded by the claims. Regarding specific arguments to claim 2, the control terminals of the first and second transistors are not positively defined as being coupled together as argued. The terminals of the input pair M11,M12 of Fattaruso are connected to the transistors read as the output stage at nodes CN1,CN2. Regarding specific arguments to claims 3-4, the sources of M13,M14 are tied together with the sources of Mf1,M21 to the voltage supply; this is the same way the (analogous) emitters of applicant's current mirror transistors are 'coupled' to the emitters of the output transistors.

Claims 10-13 are allowed. The first and second feedback resistors of claim 10 are not shown in the prior art of record in the context claimed.

Claim 5-9 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Mottola whose telephone number is 703-308-4914.

Steven J. Mottola
Primary Examiner